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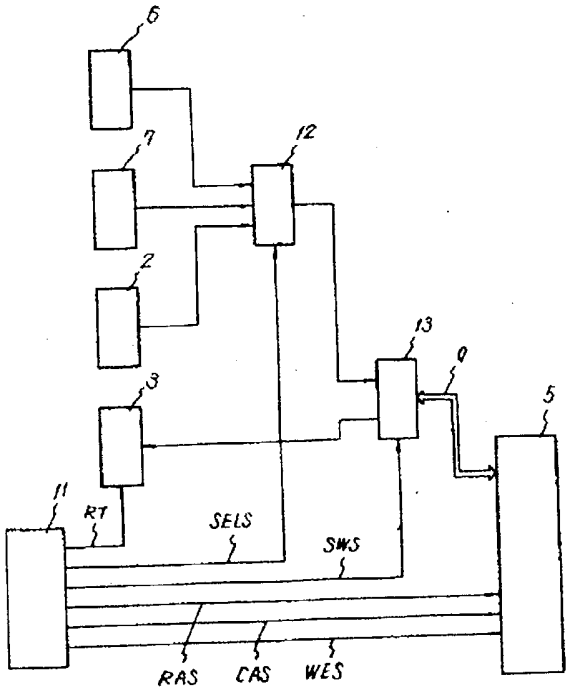
TITLE : MEMORY CONTROL SYSTEM



ABSTRACT : PURPOSE: To reduce the space of package as ICs decrease in number, and to facilitate the wiring of bus lines, by using a data bus and an address bus in common on a time-division basis when controlling the memory of a data processor.

CONSTITUTION: A control circuit 11 sends control signals and controls a readout data register 3, a selecting circuit 12, a switching circuit 13, and a memory 5. A row address register 6, a column address register 7, and a write data register 2 are selectively connected by the selecting circuit 12. The switching circuit 3 is connected to the memory 5 via a two-way bus 9 to change the bus 9 over between the circuits 3 and 12. In the start of a memory access cycle, an address is latched in the row address register in the memory 5 through the circuits 12 and 13 by a row address strobe RAS, and then latched in the column address register by a column address strobe CAS. Then, writing operation is performed by a write enable signal WES, and reading operation by readout timing RT.